Jean-Luc Gaudiot
Professor of Electrical Engineering and Computer Science
University of California, Irvine
2017 President of the IEEE Computer Society

Technology Considerations in Computer Architecture

Time: Wednesday, February 17th, 1:00pm – 2:00pm
Reception follows after the lecture
Location: Science & Engineering Hall, Lehman Auditorium B1220

Abstract

Good engineering practice makes use of the characteristics of an existing technology of implementation to best implement a system. Often, this will mean that design techniques optimal in a previous generation prove impractical or even unusable when a new technology becomes dominant. This rule of engineering is all too often forgotten and we will demonstrate it in two important problems of computer design: Field-Programmable Gate Arrays (FPGA) and hardware prefetchers. It is well known that energy efficiency is one of the most important concerns in the design of mobile embedded systems. At the same time, many embedded applications are extremely demanding in terms of computation power. While a variety of hardware techniques are available to the designer to satisfy the second constraint, these techniques are also often reputed to be power hungry. An FPGA hardware accelerator is typically used to accelerate certain parts of the program execution. When the accelerator is not active, we will show how partial reconfiguration can be used to unload the accelerator so as to reduce power consumption. However, the reconfiguration process may introduce a high energy overhead. The results of our study show that by using partial reconfiguration to eliminate the power consumption of the accelerator when it is inactive, we can accelerate program execution and at the same time reduce the overall energy consumption by half. As for hardware prefetching, we will show how technology advances (e.g., from 90 nm to 32 nm), such as prefetching start to become energy-efficient while improving performance.

Speaker Biography

Professor Jean-Luc Gaudiot received the Diplôme d'Ingénieur from ESIEE, Paris, France in 1976 and M.S. and Ph.D. in Computer Science from the University of California, Los Angeles in 1977 and 1982, respectively. He is professor of electrical engineering and computer science at the University of California, Irvine, and was department chair for 6 years. His research interests include programmability and design of multiprocessors. He has published over 250 peer reviewed papers. His research has been sponsored by NSF, DOE, DARPA, and several companies. Over the years, he has demonstrated his leadership in roles such as program committee chair or (co-) general chair of ISCA, HPCA, and PACT; editor-in-chief of IEEE Transactions on Computers; founding editor of IEEE Computer Architecture Letters; and vice president of Educational Activities (2013) and Publications (2014–2015). He has just been elected to be the 2017 President of the IEEE Computer Society. In 1999, he became a Fellow of the IEEE, “For Contributions to the Programmability and Reliability of Dataflow Architectures.” He was elevated to the rank of AAAS Fellow in 2007, “For Distinguished Contributions to the Design and Analysis of Highly Efficient Multiprocessor and Memory System Architectures.” In his spare time, Dr. Gaudiot combines his passion for aviation with his love for teaching and he is an active flight instructor (both primary and instrument).